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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/435,154	11/08/1999	SHUNPEI YAMAZAKI	SEL142	4834
7590	04/12/2006		EXAMINER	
COOK MCFARRON & MANZO LTD 200 WEST ADAMS STREET SUITE2850 CHICAGO, IL 60606			LOKE, STEVEN HO YIN	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/435,154	YAMAZAKI ET AL.
Examiner	Art Unit	
Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 23 July 2004.

2a)  This action is FINAL.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-4,6-9,11,12,14-17,19-22,24 and 25 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-4,6-9,11,12,14-17,19-22,24 and 25 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 8/29/05, 10/31/05, 12/5/05, 1/23/06  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. 20060407.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_

1. Claims 24 and 25 are objected to because of the following informalities: Claim 24, lines 22-23, the phrase "said at least one of said second source and drain regions" has no antecedent basis. Appropriate correction is required.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 14, 16, 17, 19, 21, 22, 24 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki (U.S. patent no. 6,909,114 in the IDS)

The applied reference has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regards to claim 14, Yamazaki shows all the elements of the claimed invention in figs. 12B, 31D and 32D. It is a goggle type display device (fig. 32D) having a CMOS circuit (fig. 31D) comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising: each gate electrode ([931D, 934D, 934D] of the n-channel TFT and [932D, 933D, 934D] of the p-channel TFT) of said n-channel TFT and said p-channel TFT

having a first conductive layer ([931D] in n-TFT, [933D] in p-TFT) being in contact with a gate insulating film [905], a second conductive layer ([934D] with vertical sides in n-TFT, [932D] in p-TFT) being in contact with said first conductive layer, and a third conductive layer ([934D] with slopes in n-TFT, [934D] with vertical sides in p-TFT) being in contact with said gate insulating film, side surfaces of said first conductive layer and top and side surfaces of said second conductive layer; a semiconductor layer of said n-channel TFT comprising a first channel formation region [911D], a pair of LDD regions [914D, 915D, 916D, 917D] and first source and drain regions [912D, 913D]; and a semiconductor layer of said p-channel TFT comprising a second channel formation region [921D] and second source and drain regions [922D, 923D, 924D, 925D], wherein said second conductive layer (Mo-W) comprises a different material from said first conductive layer (n-Si); wherein a portion which said third conductive layer ([934D] with slopes) is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions [914D, 915D]; wherein a portion which said third conductive layer ([934D] with vertical sides) is in contact with said gate insulating film in said p-channel TFT is partially overlaps said second source and drain regions [924D, 925D], wherein said semiconductor layer of said p-channel TFT has no LDD regions.

In regards to claim 16, Yamazaki further discloses each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer.

In regards to claim 17, Yamazaki further discloses said third conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

In regards to claim 19, Yamazaki shows all the elements of the claimed invention in figs. 12B, 31D and 32D. It is a goggle type display device (fig. 32D) having a CMOS circuit (fig. 31D) comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising: each gate electrode ([931D, 934D, 934D] of said n-channel TFT and [932D, 933D, 934D] of said p-channel TFT) of said n-channel TFT and said p-channel TFT having a first conductive layer ([931D] in n-TFT, [933D] in p-TFT) being in contact with a gate insulating film [905], a second conductive layer ([934D] with vertical sides in n-TFT, [932D] in p-TFT) being in contact with said first conductive layer, and a third conductive layer ([934D] with slopes in n-TFT, [934D] with vertical sides in p-TFT) being in contact with said gate insulating film, side surfaces of said first conductive layer and top and side surfaces of said second conductive layer; a semiconductor layer of said n-channel TFT comprising a first channel formation region [911D], a pair of LDD regions [914D, 915D, 916D, 917D] and first source and drain regions [912D, 913D]; and a semiconductor layer of said p-channel TFT comprising a second channel formation region [921D] and second source and drain regions [922D, 923D, 924D, 925D], wherein said second conductive layer (Mo-W) comprises a different material from said first conductive layer (n-Si); wherein a portion which said third conductive layer ([934D] with slopes) is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions [914D, 915D]; wherein the portion which said third conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said first source and drain regions [912D, 913D]; wherein a portion which said third conductive layer ([934D] with vertical sides) is in contact with said gate

insulating film in said p-channel TFT partially overlaps said second source and drain regions [924D, 925D], wherein said semiconductor layer of said p-channel TFT has no LDD regions.

In regards to claim 21, Yamazaki further discloses each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer.

In regards to claim 22, Yamazaki further discloses said third conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

In regards to claim 24, Yamazaki shows all the elements of the claimed invention in figs. 12B, 31D and 32D. It is a goggle type display device having an n-channel TFT and a p-channel TFT over a substrate [900], said n-channel TFT comprising: a first gate electrode ([934D] with vertical sides) and a second gate electrode ([934D] with slopes) formed adjacent to a first semiconductor layer with a first gate insulating film [905] interposed therebetween, said first semiconductor layer comprising a first channel formation region [911D], a pair of LDD regions [914D, 915D, 916D, 917D] and first source and drain regions [912D, 913D]; wherein said second gate electrode partially overlaps said pair of LDD regions while said first gate electrode does not overlap said pair of LDD regions, and wherein said second gate electrode (Ti) comprises a different material from said first gate electrode (Mo-W), and said p-channel TFT comprising: a third gate electrode [932D] and a fourth gate electrode [934D] formed adjacent to a second semiconductor layer with a second gate insulating film [905] interposed therebetween, said second semiconductor layer comprising a second channel formation

region [921D] and second source and drain regions [922D, 923D, 924D, 925D] being in contact with said second channel formation region, wherein said fourth gate electrode partially overlaps said second source and drain regions while said third gate electrode does not overlap said second source and drain regions, wherein said fourth gate electrode (Ti) comprises a different material from said third gate electrode (Mo-W) and wherein a wiring [941, 943] is connected to said at least one of said second source and drain regions.

In regards to claim 25, Yamazaki further discloses said first to fourth gate electrodes comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4, 6-9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being obvious over Yamazaki.

The applied reference has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject

matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In regards to claim 1, Yamazaki discloses a liquid crystal display device in figs. 10, 12B, 31D and 32D. The liquid crystal display having a CMOS circuit (fig. 31D) comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising: each gate electrode ([931D, 934D, 934D] of the n-channel TFT and [932D, 933D, 934D] of the p-channel TFT) of said n-channel TFT and said p-channel TFT having a first conductive layer ([931D] in n-TFT, [933D] in p-TFT) being in contact with a gate insulating film [905], a second conductive layer ([934D] with vertical sides in n-TFT, [932D] in p-TFT) being in contact with said first conductive layer, and a third conductive layer ([934D] with slopes in n-TFT, [934D] with vertical sides in p-TFT) being in contact with said gate insulating film, side surfaces of said first conductive layer and top and side surfaces of said second conductive layer; a semiconductor layer of said n-channel TFT comprising a first channel formation region [911D], a pair of LDD regions [914D, 915D, 916D, 917D] and first source and drain regions [912D, 913D]; and a semiconductor layer of said p-channel TFT comprising a second channel formation

region [921D] and second source and drain regions [922D, 923D, 924D, 925D], wherein said second conductive layer (Mo-W) comprises a different material from said first conductive layer (n-Si); wherein a portion which said third conductive layer ([934D] with slopes) is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions [914D, 915D]; wherein a portion which said third conductive layer ([934D] with vertical sides) is in contact with said gate insulating film in said p-channel TFT is partially overlaps said second source and drain regions [924D, 925D], wherein said semiconductor layer of said p-channel TFT has no LDD regions.

Yamazaki differs from the claimed invention by not showing the liquid crystal is ferroelectric liquid crystal. It would have been obvious for the liquid crystal is ferroelectric liquid crystal, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

In regards to claim 3, Yamazaki further discloses each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer.

In regards to claim 4, Yamazaki further discloses said third conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

In regards to claim 6, Yamazaki discloses a liquid crystal display device in figs. 10, 12B, 31D and 32D. The liquid crystal display having a CMOS circuit (fig. 31D) comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising: each gate electrode ([931D, 934D, 934D] of said n-channel TFT and [932D, 933D, 934D] of

said p-channel TFT) of said n-channel TFT and said p-channel TFT having a first conductive layer ([931D] in n-TFT, [933D] in p-TFT) being in contact with a gate insulating film [905], a second conductive layer ([934D] with vertical sides in n-TFT, [932D] in p-TFT) being in contact with said first conductive layer, and a third conductive layer ([934D] with slopes in n-TFT, [934D] with vertical sides in p-TFT) being in contact with said gate insulating film, side surfaces of said first conductive layer and top and side surfaces of said second conductive layer; a semiconductor layer of said n-channel TFT comprising a first channel formation region [911D], a pair of LDD regions [914D, 915D, 916D, 917D] and first source and drain regions [912D, 913D]; and a semiconductor layer of said p-channel TFT comprising a second channel formation region [921D] and second source and drain regions [922D, 923D, 924D, 925D], wherein said second conductive layer (Mo-W) comprises a different material from said first conductive layer (n-Si); wherein a portion which said third conductive layer ([934D] with slopes) is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions [914D, 915D]; wherein the portion which said third conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said first source and drain regions [912D, 913D]; wherein a portion which said third conductive layer ([934D] with vertical sides) is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions [924D, 925D], wherein said semiconductor layer of said p-channel TFT has no LDD regions.

Yamazaki differs from the claimed invention by not showing the liquid crystal is ferroelectric liquid crystal. It would have been obvious for the liquid crystal is ferroelectric liquid crystal, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

In regards to claim 8, Yamazaki further discloses each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer.

In regards to claim 9, Yamazaki further discloses said third conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

In regards to claim 11, Yamazaki discloses a liquid crystal display device in figs. 10, 12B, 31D and 32D. The liquid crystal display having an n-channel TFT and a p-channel TFT over a substrate [900], said n-channel TFT comprising: a first gate electrode ([934D] with vertical sides) and a second gate electrode ([934D] with slopes) formed adjacent to a first semiconductor layer with a first gate insulating film [905] interposed therebetween, said first semiconductor layer comprising a first channel formation region [911D], a pair of LDD regions [914D, 915D, 916D, 917D] and first source and drain regions [912D, 913D]; wherein said second gate electrode partially overlaps said pair of LDD regions while said first gate electrode does not overlap said pair of LDD regions, wherein said second gate electrode comprises a different material (Ti) from said first gate electrode (Mo-W), and said p-channel TFT comprising: a third gate electrode [932D] and a fourth gate electrode [934D] formed adjacent to a second semiconductor

layer with a second gate insulating film [905] interposed therebetween, said second semiconductor layer comprising a second channel formation region [921D] and second source and drain regions [922D, 923D, 924D, 925D] being in contact with said second channel formation region, wherein said fourth gate electrode partially overlaps said second source and drain regions while said third gate electrode does not overlap said second source and drain regions, wherein said fourth gate electrode (Ti) comprises a different material from said third gate electrode (Mo-W) and wherein a wiring [941, 943] is connected to said at least one of said second source and drain regions.

Yamazaki differs from the claimed invention by not showing the liquid crystal is ferroelectric liquid crystal. It would have been obvious for the liquid crystal is ferroelectric liquid crystal, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

In regards to claim 12, Yamazaki further discloses said first to fourth gate electrodes comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

In regards to claims 2, 7, 15, 20, Yamazaki differs from the claimed invention by not showing said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

It would have been obvious for the first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium

(Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

In addition, it would have been obvious for the first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo) because they are widely used low resistance and high-melting point gate material.

6. Applicant cannot rely upon the foreign priority papers to overcome the above prior art rejections because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 7, 2006

Steven Loke  
Primary Examiner  
